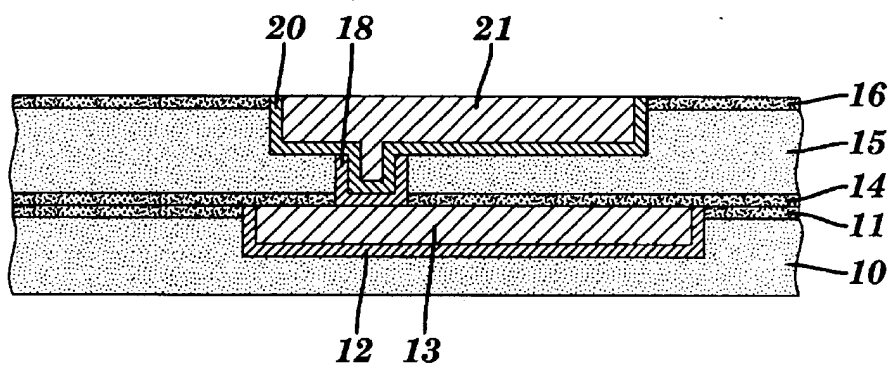
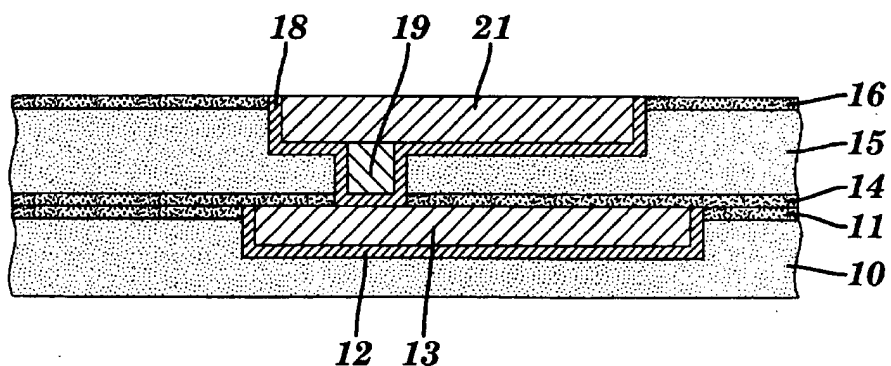
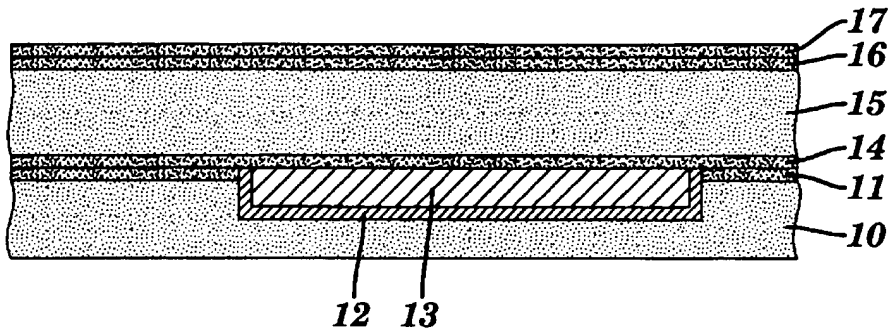


**FIG. 1**

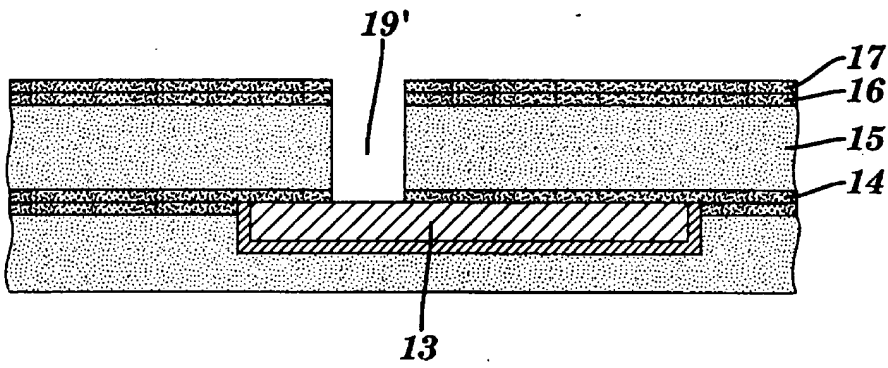


**FIG. 2**

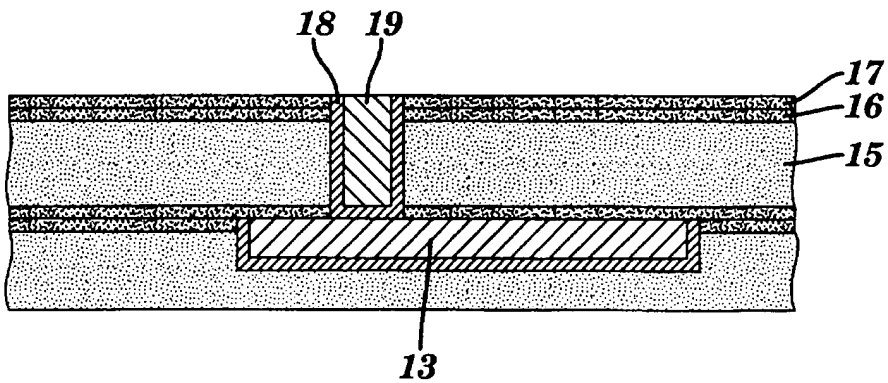




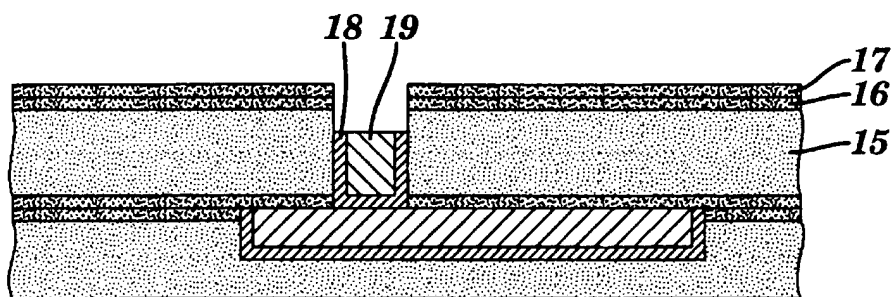
**FIG. 4(a)**



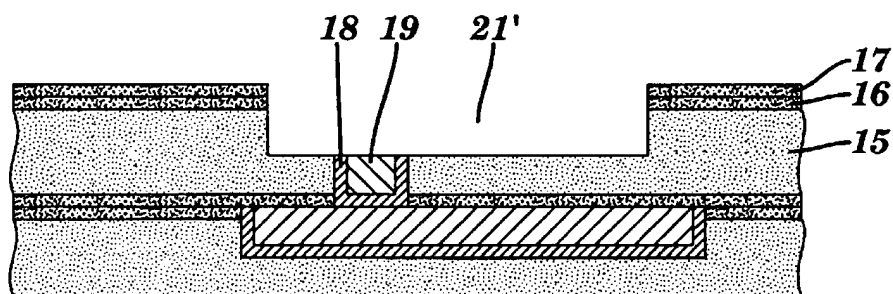
**FIG. 4(b)**



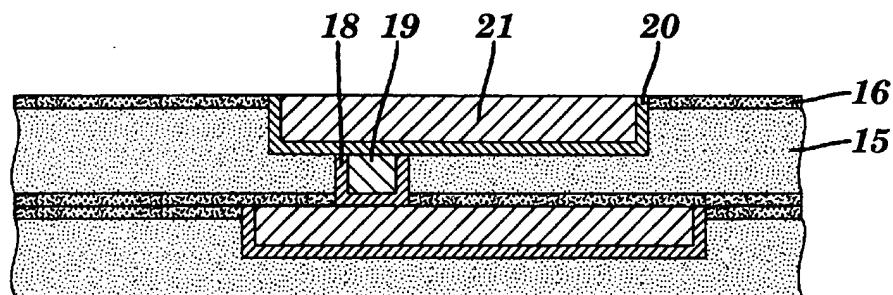
**FIG. 4(c)**



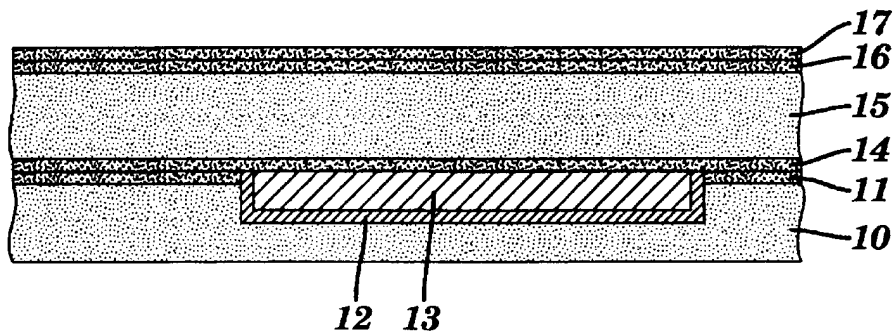
**FIG. 4(d)**



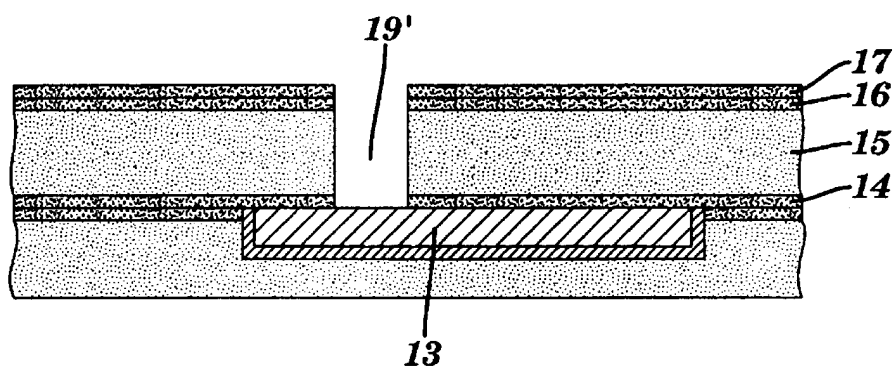
**FIG. 4(e)**



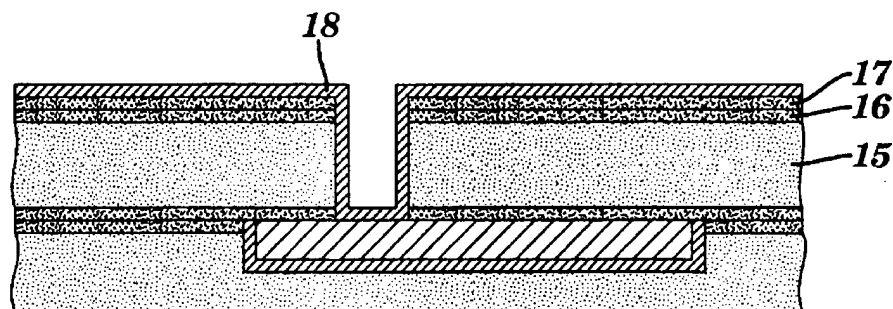
**FIG. 4(f)**



**FIG. 5(a)**



**FIG. 5(b)**

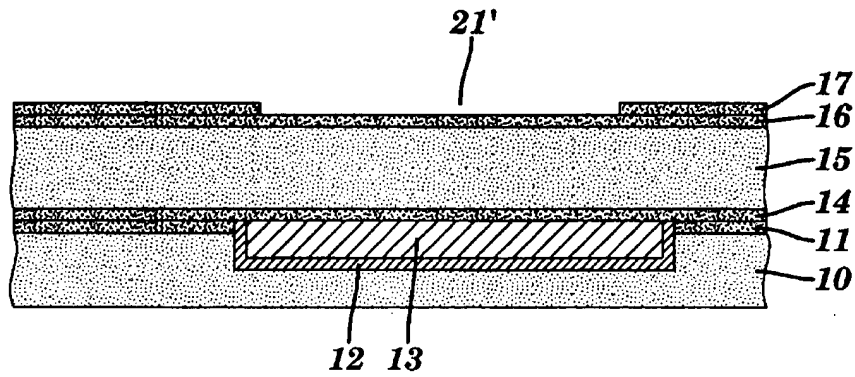


**FIG. 5(c)**

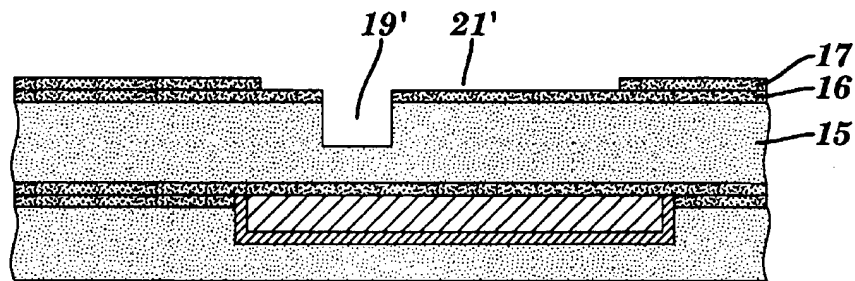
Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 15 with a thin layer 16 and a top layer 17. A central region 18 is defined by a trench 19' and a raised region 21'.

A cross-sectional view of a semiconductor device. It shows a substrate 15 with a thin layer 16 on top. A patterned layer 20 is formed on the substrate, with a central structure 18. The structure 18 is formed by a series of steps, and a top layer 21 is formed on top of it.

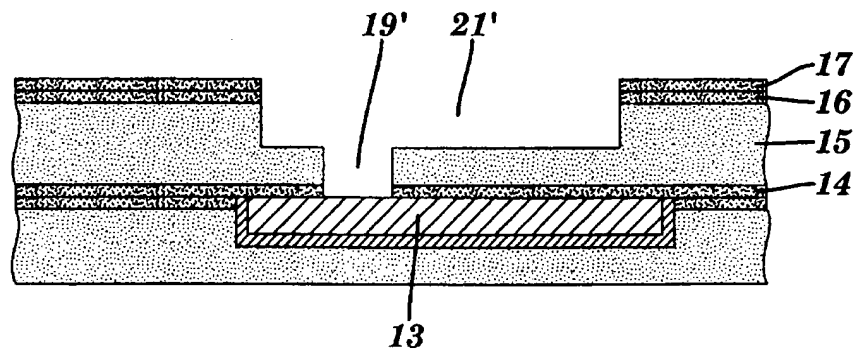
**FIG. 5(f)**



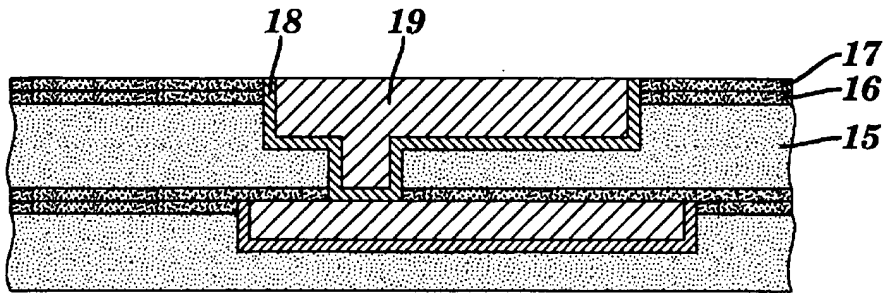
**FIG. 6(a)**



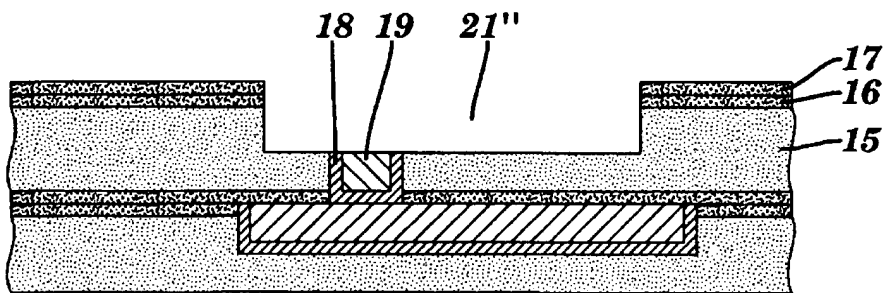
**FIG. 6(b)**



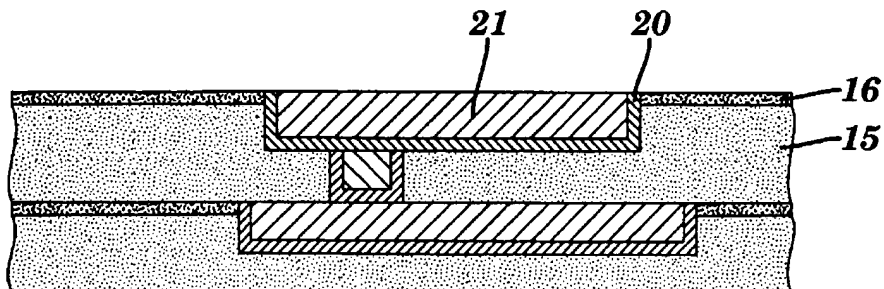
**FIG. 6(c)**



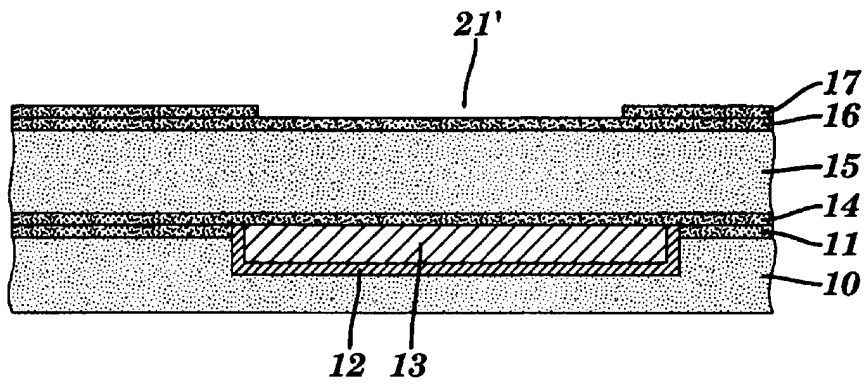
**FIG. 6(d)**



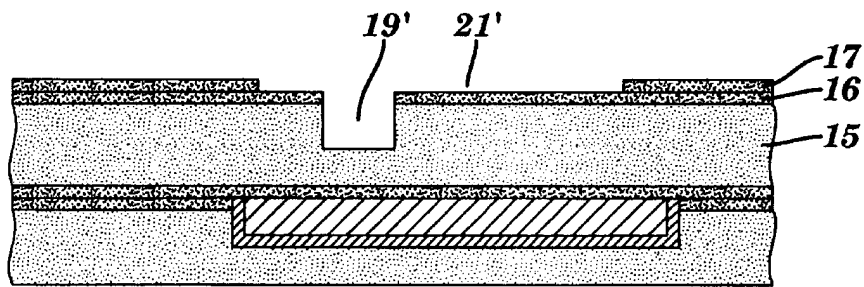
**FIG. 6(e)**



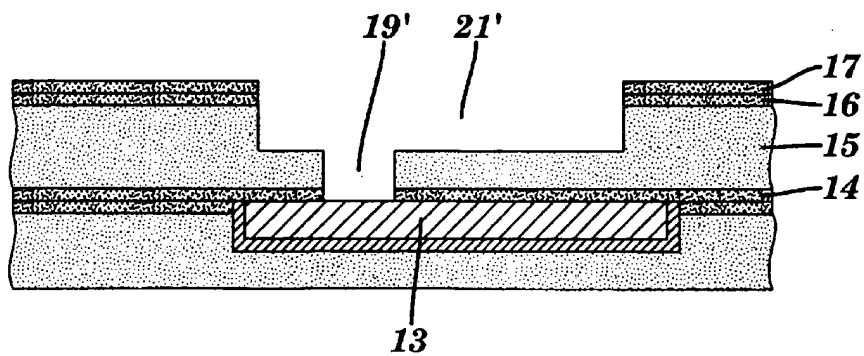
**FIG. 6(f)**



**FIG. 7a)**

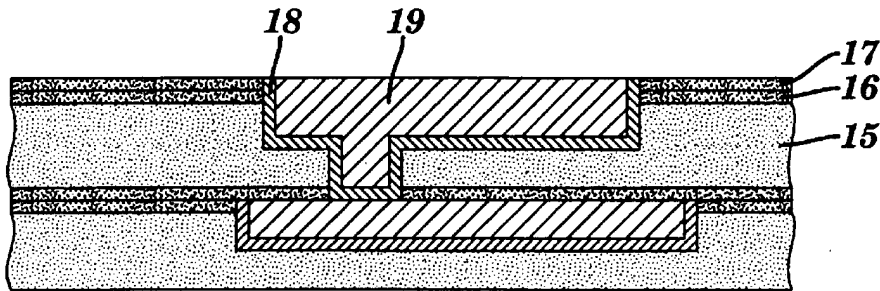


**FIG. 7(b)**

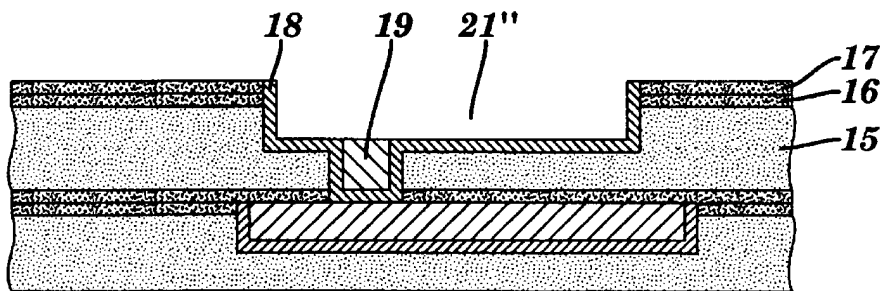


**FIG. 7(c)**

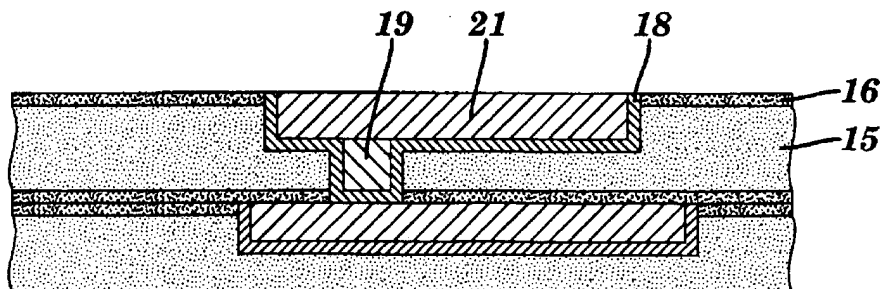




**FIG. 7(d)**



**FIG. 7(e)**



**FIG. 7(f)**

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